AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (canceled)

2. (currently amended) The semiconductor integrated circuit according to claim [[1]] 31, wherein at least one of said power supply ~~line is extended~~ lines extends ~~in wiring~~ to be connected to an external connection terminal.

3. (currently amended) The semiconductor integrated circuit according to claim [[1]] 31, further comprising a mutual connection line for connecting together some of said power supply lines having equal potentials, wherein the mutual connection line is not connected to any of said power supply lines other than those having equal potentials.

4. (currently amended) The semiconductor integrated circuit according to claim [[1]] 31, wherein the area occupied by all of said power supply lines is larger than the area occupied by all of the regions between said power supply lines.

5. (withdrawn/currently amended) The semiconductor integrated circuit according to claim [[1]] 31, further comprising a gate signal wiring line in order to avoid a delay of a gate signal propagating through the corresponding one of the gate electrodes of said transistors, the gate signal wiring line having a resistance and a parasitic capacitance lower than those of the gate electrode.

6. (canceled)

7. (canceled)

8. (withdrawn, currently amended) A charge pump circuit comprising the semiconductor integrated circuit according to claim [[1]] 31, and a configuration of a plurality of capacitors and a plurality of transistors.

9-15. (canceled)

16. (withdrawn) A semiconductor integrated circuit comprising a structure in which source, drain and gate electrodes of transistors included in a circuit are placed in a small-width region having a width determined from the number of routes in a set of routes having the smallest number of routes in sets of routes formed so that passage through any one of the transistors

included in the circuit occurs only one time and so that the combination of routes in one set can cover the entire circuit network of the circuit, determined from the widths of source and drain electrodes of each transistor, determined from the width of the region between the source and drain electrodes, determined from the width of the region between the source or drain electrodes of some of the adjacent pairs of the transistors not combined into a common electrode, and determined from the number of the transistors included in the circuit.

17. (withdrawn) The semiconductor integrated circuit according to claim 16, wherein if the width of the source and drain electrodes of each transistor is Wi; the width of the region between the source and drain electrodes is Lj; the width of the region between the source or drain electrodes of some of the adjacent pair of transistors not combined into a common electrode is Pk; the number of the transistors is n; and the number of routes included in the set of routes having the smallest number of routes is m, said small-width region has a width expressed by the following expression:

$$\sum_{i=1}^{n+m} Wi + \sum_{j=1}^{n} Lj + \sum_{k=1}^{m-1} Pk$$

18. (withdrawn) The semiconductor integrated circuit according to claim 16, wherein the width of the region between

the source or drain electrodes of some of the adjacent pair of transistors not combined into a common electrode is smaller than the width of the region between the source and drain electrodes.

19. (withdrawn) The semiconductor integrated circuit according to claim 16, wherein the source/drain electrodes and the gate electrodes are alternately placed in correspondence with each of the routes in an arbitrary one of the at least one set of routes having the smallest number of routes in the order of passage through the transistors designated with the route or in the order reverse to the passage order.

20. (withdrawn) The semiconductor integrated circuit according to claim 16, wherein the source/drain electrodes and the gate electrodes are alternately placed in accordance with a set of routes having the shortest entire length of mutual wiring for connecting together some of the source or drain electrodes having equal potentials in the sets of routes having the smallest number of routes, in accordance with the order of the plurality of routes contained in the set of routes, and in accordance with the connection direction of each route and the connection direction of each route contained in the set of route.

21. (withdrawn) The semiconductor integrated circuit according to claim 19, wherein some of the source or drain

electrodes having equal potentials are connected to each other by a mutual connection line which extends across the source or drain electrodes.

22. (withdrawn) The semiconductor integrated circuit according to claim 19, wherein at least one of the source and drain electrodes of the transistors to be connected to an external terminal is extended for connection to the external terminal.

23. (withdrawn) The semiconductor integrated circuit according to claim 16, wherein said transistors are thin-film transistors formed on a glass substrate or an insulation substrate other than a semiconductor substrate.

24-30. (canceled)

31. (new) A semiconductor integrated circuit comprising:

at least three power supply lines; and

at least two transistors for switching between said at least three power supply lines,

wherein first, second and third power supply lines of said at least three power supply lines are arranged side-by-side in that order,

wherein said at least two transistors include first and second transistors respectively placed in a gap between said first and second power supply lines and a gap between said second and third power supply lines, said first and second transistors being formed on opposite sides of said second power supply line,

wherein said first and second transistors are thin-film transistors on an insulation substrate other than a glass substrate or a semi-conductor substrate, and

wherein said first transistor switches between said first and second powers supply lines and said second transistor switches between said second and third powers supply lines.

32. (new) A semiconductor integrated circuit, comprising:

at least three power supply lines; and

at least two transistors for switching between said at least three power supply lines,

wherein first, second and third power supply lines of said at least three power supply lines are arranged side-by-side in that order,

wherein said at least two transistors include first and second transistors respectively placed in a gap between said first and second power supply lines and a gap between said second and third power supply lines, said first and second transistors being formed on opposite sides of said second power supply line,

wherein at least one of said at least three power supply lines extends straight to an external connection terminal and is connected to said external connection terminal.